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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TODD P. LUKANC, CYRUS E. TABERY, LUIGI CAPODIECI, CARL BABCOCK, HUNG-EIL KIM, CHRISTOPHER A. SPENCE, and CHRIS HAIDINYAK

Appeal 2008-3655
Application 10/790,590
Technology Center 2800

Decided: November 20, 2008

Before JOHN C. MARTIN, JOSEPH F. RUGGIERO, and JOHN A. JEFFERY, *Administrative Patent Judges.*

MARTIN, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-4, 6-20, and 31, all of the pending claims, under 35 U.S.C. § 103(a).

We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

A. Appellants' invention

Appellants' invention relates generally to the field of integrated circuit device design and manufacture and, more particularly, to a system and method for designing an integrated circuit device that employs a simulation tool. Specification 1:1-5.

As explained below, Figures 3 and 4 show first and second embodiments of Appellants' invention, while Figure 6 shows a third embodiment that combines the first and second embodiments.

Appellants' Figure 3 is reproduced below.

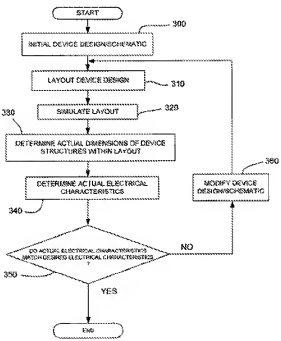

FIG. 3

Figure 3 is a flow chart illustrating a method of designing an integrated circuit (IC) device in accordance with a first embodiment of Appellants' invention (*id.* at 7:13-14).

At step 300, an initial circuit design or schematic is provided by a designer, for example as a "netlist" (*id.* at 7:17-25).

At step 310, the IC device design is converted into a physical layout or polygonal representation (*id.* at 7:26-27). The generated layout representation can define the specific dimensions of the gates, isolation regions, interconnects, contacts, and other device elements that form the physical structures within the device design (*id.* at 7:27-30).

At step 320, the layout is simulated (*id.* at 8:15). In other words, the real pattern of the structures within the device design is simulated as a result of one or more of resolution enhancement technologies, optical proximity correction (OPC), proximity to other structures, density, corner rounding, as well as any other parameters that alter the final image (i.e., the wafer image) as compared to the drawn layout or polygonal representation (*id.* at 8:15-20). The layout can be simulated using one of a variety of commercially available simulation tools that are useful for simulating or otherwise predicting how the structures within the device design will actually pattern and/or what manufacturing defects will occur during lithographic processing (*id.* at 8:20-25).

At step 330, the designer or other operator can determine the actual dimensions of the structures within the IC device layout by using a

simulation tool to better understanding how things will actually pattern on the wafer (*id.* at 8:26-29).

At step 340, the actual electrical characteristics associated with the IC device design are determined using the actual dimensions of the structures within the IC determined from the simulated layout (steps 320, 330) (*id.* at 9:5-8).

At step 350, the actual electrical characteristics associated with the initial IC device design are compared to desired electrical characteristics for the device design (*id.* at 9:18-20). The electrical characteristics can include any or all of resistance, gain, switching speed, drive current, and the like (*id.* at 9:20-21), of which gain and switching speed are recited in each of claims 1 and 31. If the actual electrical characteristics sufficiently match the desired electrical characteristics and/or are within the specifications set by the designer, the method illustrated in Figure 3 ends (*id.* at 9:26-29). If the actual electrical characteristics do not sufficiently match the desired electrical characteristics and/or are not within the performance specifications set by the designer, the device design or schematic can be modified (step 360) in order to achieve the desired electrical characteristics and/or performance specifications and the method described above can be repeated (*id.* at 10:1-6).

Appellants' Figure 4 is reproduced below.

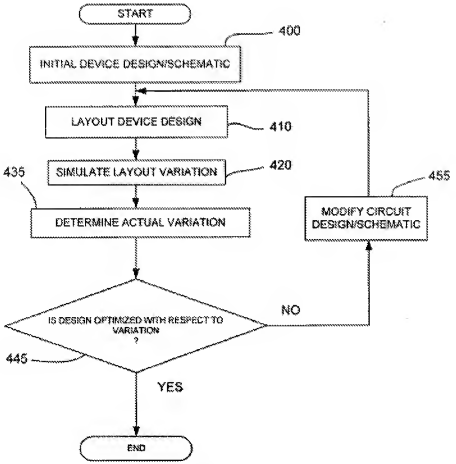

FIG. 4

Figure 4 is a flow chart depicting another embodiment of Appellants' invention (*id.* at 10:10-11).

This embodiment involves a determination of "variations" rather than dimensions.

At step 410, the IC device design (typically in the form of a netlist)

can be converted into a physical layout or polygonal representation (*id.* at 11:1-2).

At step 420, the layout and pattern variations contained therein can be simulated using one of a variety of commercially available simulation tools (*id.* at 11:10-12). By using such a simulation tool, some or all of the parameters impacting process-related or lithography-related variation can be simulated (*id.* at 11:13-15). Parameters that impact the variation in how a structure or cell will print on the wafer include, but are not limited to, proximity to other structures and/or cells, density of structures, orientation of structures, placement, and size with respect to other structures on the same GDS[1] level or other levels (*id.* at 11:15-18). These variations can result from a number of factors, including mask generation (including pattern write variations and stray light, resist variations, etch variations, and other parameters that contribute to critical dimension (CD) variation), wafer patterning (including write variations, exposure and focus variation, resist thickness and property variation and other parameters that contribute to CD variations), and pre- / post-patterning processing (such as etch, deposition, polish and need to take into account aspects like topography, spin coating, variations in film thickness and property variations, and other processing steps that can impact a particular layer's patterning) (*id.* at 11:18-27).

[1] Typical formats for the polygons of a layout are GDS II or CIF (Specification at 8:11).

At step 435, the actual variation between two or more structures within a design can be determined based on the simulation of step 420 (*id.* at 11:28-29). Using this methodology, a designer can learn the actual variation of one or more structures of interest and, therefore, avoid over-guard banding a design (i.e., avoid designing to a worst case scenario when that is unnecessary) (*id.* at 11:31 to 12:2).

As discussed below, steps 420 and 435 can be implemented by simulating the slopes of the illumination intensity at edges of structures within the design (*id.* at 12:3-5).

Figures 5A and 5B are reproduced below.

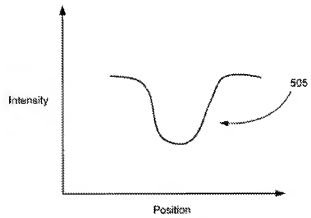

FIG. 5A

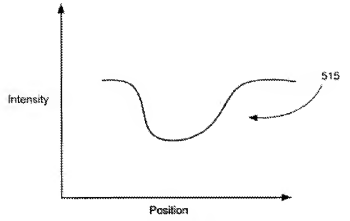

FIG. 5B

Figures 5A and 5B illustrate "exemplary plots of intensity versus position corresponding to structure edges simulated in accordance with the present invention" (*id.* at 4:16-18).

Based on a determination of the slope of the illumination intensity or logarithm of the slope, the amount of process-related variation in a particular structure can be determined (*id.* at 12:5-6). For example, the slope of edge 505 in Figure 5A is much greater than the slope of edge 515 in Figure 5B (*id.* at 12:12-13). Based on this information, it can be determined that the edge 505 depicted in Figure 5A can withstand much more process variation then the edge 515 depicted in Figure 5B (*id.* at 12:14-16). In other words, a given amount of process variation will cause a relatively small change in critical dimension (CD) for the edge 505 than for the edge 515 (*id.* at 12:16-18). The actual variation can be determined using a software-based or otherwise computer-implemented lookup table that references edge intensity slope and variation of process parameters (*id.* at 12:20-22). Using the slope

of edge intensity to determine process-related variation is recited in claims 10 and 11.

At step 445, the actual variation between given structures is used to evaluate whether or not the overall device design or portions thereof is optimized with respect to process variation (*id.* at 12:23-25). For example, it may be determined that a certain structure built with a certain proximity to other structures and overall density may have a much smaller process variation than designed for in design step 400 and layout step 410 (*id.* at 12:25-28). If it is determined that the design is not optimized with respect to variation, the design can be modified appropriately at step 455 (*id.* at 12:28-30). Such optimization can include adjustment of one or more of proximity to other structures and/or cells, density of structures, orientation of structures, placement, and size with respect to other structures on the same GDS level or other levels (*id.* at 12:30 to 13:2).

Metrics other than the slope of edge intensity can be employed for determining process-related variation, such as maximum intensity in a region to be exposed away, minimum intensity in a region not to be exposed, simulated edge placement with respect to the target pattern, how movement of other edges impacts the edge being checked, and the like (*id.* at 13:12-18).

In one embodiment, any or all of the aforementioned metrics can be evaluated over a range of focus and intensity (i.e., over a process window) to determine whether an undesired effect begins to occur as the focus and

intensity move away from the "best settings" (*id.* at 13:19-23). This aspect of the invention is the subject of claim 12.

Figure 6 is reproduced below.

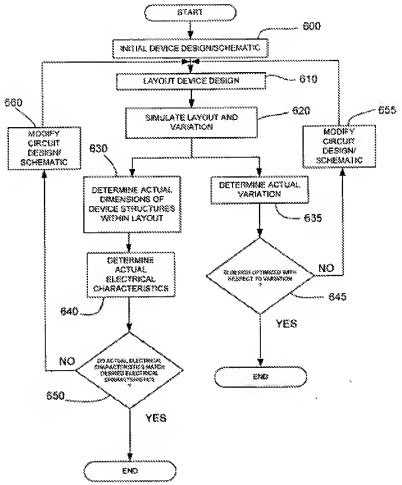

FIG. 6

Figure 6 is a flow chart depicting yet another embodiment of the invention (*id.* at 13:24-25).

The method employed in the Figure 6 embodiment is a combination of the methods employed in the Figure 3 and Figure 4 embodiments, which

methods essentially act in parallel, as is apparent from a comparison of the three figures.

B. The claims

The independent claims before us are claims 1 and 31, of which claim 1 reads:

> 1. A method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:
>
> providing an initial IC device design;
>
> generating a layout representation corresponding to the initial IC device design;
>
> simulating how structures within the layout representation will pattern on a wafer;
>
> based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics, wherein the desired electrical characteristics include at least one of gain and switching speed; and
>
> if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design.

Claims App., Br. 23.[2]

The recitation of determining actual electrical characteristics in claim 1 suggests that it is directed to the embodiment depicted in Figure 3, which is also part of the third embodiment depicted in Figure 6.

[2] All references hereinafter to the language of the claims are to the (Continued on next page.)

C. The references and rejections

The Examiner relies on the following references:

Rosenbluth et al. (Rosenbluth)	US 2002/0140920 A1	Oct. 3, 2002
White et al. (White)	US 2003/0229868 A1	Dec. 11, 2003
Hatsch et al. (Hatsch)	US 6,735,742 B2	May 11, 2004

Claims 1-4, 6-9, 12-18, 20, and 31 stand rejected under 35 U.S.C. § 103(a) for obviousness over White in view of Hatsch.

Claims 10, 11, and 19 stand rejected under § 103(a) for obviousness over White in view of Hatsch and Rosenbluth.

THE ISSUE

Generally speaking, the issue is whether Appellants have shown reversible error by the Examiner in maintaining the rejections. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Regarding independent claims 1 and 31, Appellants argue that the Examiner erred in concluding it would have been obvious in view of Hatsch

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claims as reproduced in the Claims Appendix (Br. 23-26).

to modify White so as to use gain or switching speed to evaluate the electrical characteristics of the simulated structures. Appellants also separately argue the limitations recited in a number of the dependent claims.

ANALYSIS

A. Principles of law

Application claims are interpreted as broadly as is reasonable and consistent with the specification, taking into account any definitions given in the specification. *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). A rejection under 35 U.S.C. § 103(a) must be based on the following factual determinations: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)).

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Leapfrog Enter., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (quoting *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739 (2007).

Discussing the obviousness of claimed combinations of elements of prior art, *KSR* explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.,* 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co*., 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. If the claimed subject matter "involve[s] more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement," *id.*,

> it will be necessary . . . to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

Id. at 1740-41. "To facilitate review, this analysis should be made explicit." *Id.* at 1741. That is, "there must be some articulated reasoning with some

rational underpinning to support the legal conclusion of obviousness." *Id.* (quoting *Kahn*, 441 F.3d at 988).

The rationale for combining reference teachings is not limited to the problem the applicant was trying to solve, as "any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *In re ICON Health and Fitness Inc.*, 496 F.3d 1374, 1380 (Fed. Cir. 2007) (quoting *KSR*, 127 S. Ct. at 1742).

Also, a rationale for combining or modifying reference teachings can be based on common knowledge or common sense rather coming from the references themselves. "[T]he [obviousness] analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 127 S. Ct. at 1741. As explained in *Dystar*,

> an implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the "improvement" is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.

464 F.3d at 1368. *See also Leapfrog,* 485 F.3d at 1162 (holding it "obvious to combine the Bevan device with the SSR to update it using modern electronic components in order to gain the commonly understood benefits of

such adaptation, such as decreased size, increased reliability, simplified operation, and reduced cost").

Furthermore, a reference may be understood by the artisan to be suggesting a solution to a problem that the reference does not discuss. *See KSR*, 127 S. Ct. at 1742 ("The second error of the Court of Appeals lay in its assumption that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem. . . . Common sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton.").

B. The merits of the rejection based on White in view of Hatsch

White discloses a method of designing an integrated circuit that addresses the fact that "pattern dependencies between the process by which the ICs are fabricated and the pattern that is being created often cause processed films to have significant variation in thickness across a surface, resulting in variation in feature dimensions (e.g. line widths) of integrated circuits (ICs) that are patterned using the mask" (White at [0003]).

Many projection systems use step-and-repeat mechanisms that expose only a sub-area of the wafer or a die, also referred to as the optical field, and then repeat the process until the entire wafer is imaged (*id.* at [0119]). The

stepper may be controlled to accommodate wafer-level variation that occurs across the wafer as a result of, for example, warp or bow (*id.*). This technique is normally used to accommodate variability that occurs from die to die, but not variability that occurs within each die (*id.*).

White's Figure 3 is reproduced below.

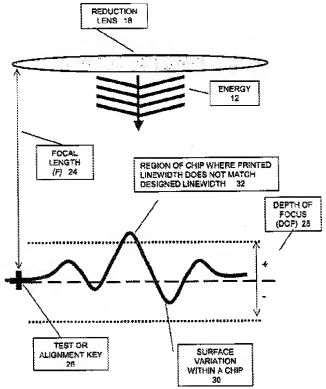

Fig. 3

Figure 3 illustrates a case in which the focal distance to an alignment key is proper, but chip-level variation is outside the depth of focus limits (*id.* at [0018]).

White's Figure 6A is reproduced below.

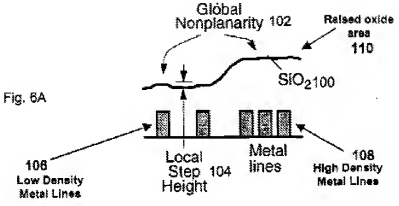

Figure 6A illustrates the film thickness variation caused by oxide chemical mechanical polishing (CMP) (*id.* at [0021]).

For oxide polishing, the major source of variation is caused by within-die pattern density variation 102, shown as two groups of metal lines in Figure 6A (*id.* at [0127]). The metal lines 106 on the left side of Figure 6A have a lower density in the direction of the plane of the integrated circuit than do the metal lines 108 on the right side of the figure (*id.*). A higher underlying feature density leads to larger film thickness, while a lower underlying feature density leads to a reduced film thickness (*id.* at [0128]).

White's Figure 8 is reproduced below.

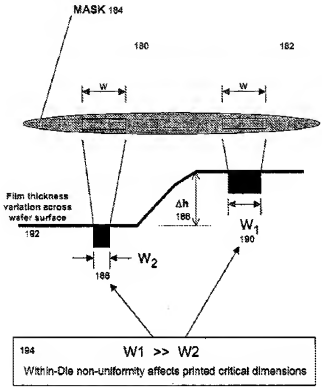

Fig. 8

Figure 8 illustrates how surface topography (i.e., film thickness variations) can affect printed feature dimensions (*id.* at [0026]).

Although both line widths 180 and 182 on the mask have the same dimensions, the surface level non-uniformity can result in significantly different dimensions in the printed features 188 and 190, which can affect the performance of the manufactured IC (*id.* at [0132]).

White's Figure 9 is reproduced below.

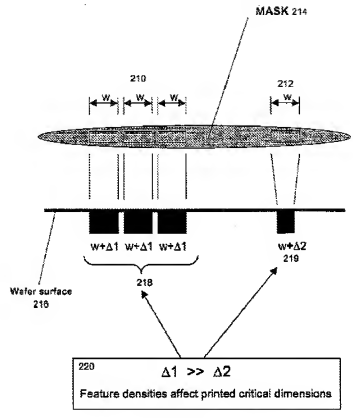

Fig. 9

Figure 9 illustrates how feature density can affect printed feature dimensions even in the absence of film thickness variation (*id.* at [0133]).

As shown in this figure, "[a]s features on the chip are placed closer to each other (i.e., feature density increases), the diffraction patterns associated with them change[,] often resulting in a feature dimension that varies from that designed" (*id.* at [0133]). Thus, even with a perfectly planar wafer surface across the chip 216, the printed feature dimensions (e.g., line widths) $w+\Delta 1$ and $w+\Delta 2$ may vary from the dimensions designed and patterned on the mask (*id.*).

Electrical extraction and simulator components may be used to assess the electrical impact of variations in features (e.g. width, height, depth, sidewall angle) across the chip and fine-tune the specified tolerances for the chip (*id.* at [0135]). The electrical impact of feature width variation can be evaluated by performing full-chip or critical circuit network simulation using resistance-capacitance (RC) extraction and other electrical simulation tools, thereby allowing for examination of issues related to interconnect feature width variation, such as coupling capacitance, noise and timing (*id.* at 0144]).

The physical characteristics (e.g. total copper loss, dishing and erosion) and electrical characteristics (e.g. sheet rho variation, timing closure, signal integrity, power grid and overall performance) are checked against specifications for the device (*id.*). The verification step weighs the results and either passes or rejects this design level. If the design passes, the original design file is used for mask creation 228 (*id.*). If the design is rejected or fails to pass, both the feature width and topographical variation results are provided to the designer or may be input into a design or mask correction component 229 (*id.*). In correction step 237 (Fig. 10C), the design file is modified so that the mask features compensate for width variation (*id.* at [0145]).

Appellants do not challenge the Examiner's finding that White satisfies all of the limitations of claim 1 with the exception of the requirement that "the desired electrical characteristics include at least one of

gain and switching speed." *See* Answer 4 ("White does not specifically disclose that desired electrical characteristics include at least one of only gain and switching activity."). For such a teaching, the Examiner relies on Hatsch.

Before addressing Hatsch, we note that the Examiner reads the remaining limitations of claim 1 on White as follows. The Examiner reads the first step ("providing an initial IC device design") on block 36 in Figure 2, which block is described as representing a computer-aided-design (CAD) system that is used to translate a functional circuit design into an electronic layout design file that represents a physical device, layer-by-layer (*id.* at [0118]). Answer 3.

The Examiner reads the second step ("generating a layout representation corresponding to the initial IC device design") on element 36 in Figure 2 as well as on Figures 10A-10C, of which Figure 10A describes the basic flow for design verification and for mask correction, while Figures 10B and 10C provide more detailed flows for design verification and mask correction, respectively (*id.* at [0144]). Answer 3. In Figure 10A, the relevant block is 280 ("Layout Generation") and in Figure 10B it is block 221 ("Generate Layout for Interconnect Level *N*").

The Examiner reads the third step ("simulating how structures within the layout representation will pattern on a wafer") on Figures 10B and 10C. Answer 3. In Figure 10B, the relevant block is 224, which represents modification of a temporary design file to reflect the feature width variation

that will result from the lithography (and optionally, the plasma etch) process (*id.* at [0144]).

As for the fourth step, the Examiner (Answer 3) reads the language "based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics" on paragraph [0144], which explains that the physical characteristics (e.g. total copper loss, dishing and erosion) and electrical characteristics (e.g. sheet rho variation, timing closure, signal integrity, power grid and overall performance) are checked (block 226) against the specifications for the device.

Finally, the Examiner (Answer 4) reads the last step of claim 1 ("if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design") on several paragraphs in White, including paragraph [0144], which explains that "[i]f the design is rejected or fails to pass, both the feature width and topographical variation results are provided to the designer or may be input into a design or mask correction component 229 . . . ."

Hatsch discloses a method for optimizing the cell layout and the cell arrangement on an integrated semiconductor (Hatsch, col. 1, ll. 9-11).

Hatsch's method is an improvement on the prior-art method discussed in the "Background of the Invention" (Hatsch, cols. 1-4). The prior-art design method begins with the creation of a cell-based network list (CBN)

(*id.* at col. 1, ll. 23-25), a cell being a unit of functionally associated components or cells (*id.*, col. 1, ll. 31-34). The CBN is a hierarchically structured list of all the cells used for the circuit and the connections between the cells (*id.* at col. 1, ll. 29-30). In addition to designators and connections, the CBN contains references to a standard cell library that contains many standard cells, for example an inverter, in various manifestations which differ in terms of their driver capability and thus also in terms of the size, number, and arrangement of the components situated in the cell (*id.* at col. 1, l. 64 to col. 2, l. 3).

The next step in the prior art design method is to calculate a layout (*id.* at col. 2, l. 11) by arranging the cells defined in the CBN next to one another and the connection of the terminal contacts of the cells in accordance with the specifications of the CBN (*id.* at col. 2, ll. 18-22).

Next, in order to be able to use a so-called simulator to check the functional capability of the layout, a network list containing information about the electrical elements used in the layout is created from the layout by means of an extraction program (*id.*, col. 2, ll. 59-63). The network list includes information about the arrangement and the appearance of the individual cells, but also contains further-reaching information, for example about the components used in the cells, expected capacitive coupling between two or more interconnects, and information about the influence on adjacent components (*id.*, col. 2, l. 65 to col. 3, l. 4).

The simulation uses given physical and electrical laws to test whether the layout of the integrated circuit and the circuit itself correspond to the requirements (*id.*, col. 3, ll. 11-14). If the requirements are not met, the circuit can be changed by exchanging specific cells which, for example, have a higher driver capability (*id.*, col. 3, ll. 14-16). Sometimes, although the cells used are strong enough to satisfy the requirements imposed, they are overdimensioned, which results in the circuit consuming too much current and producing more heat (*id.*, col. 3, ll. 19-23).

Hatsch's "Background of the Invention" also describes the optimization programs that have been used to optimize the circuit according to predetermined parameters (power, area, speed) (*id.*, col. 3, ll. 27-30). These programs define the simulated currents within the simulated semiconductor and usually determine a so-called critical path, which is an electrical conductor or signal path between a specific input of the circuit and an output of the circuit which turns out to be the worst signal path according to predetermined optimization parameters (*id.*, col. 3, ll. 30-36). By way of example, if the circuit is to be optimized according to the optimization parameter of speed, the critical path is that path through the circuit which is the slowest, that is to say has the longest propagation time from the input of a signal at the input of the circuit until the appearance of an output signal at an output of the circuit (*id.*, col. 3, ll. 36-43).

After the critical path of the circuit has been ascertained, a causality ascertainment is carried out, in which the critical cell(s) in the critical path is

or are identified (*id.*, col. 3, ll. 52-54). In a subsequent step, the dimensions of the components of the cells assessed as critical are adapted until the critical path exhibits an improved behavior and no longer represents that path having the worst behavior of all possible paths within the circuit and the semiconductor (*id.*, col. 3, ll. 54-59). This optimization method is applied a number of times to the circuit to be examined, or the semiconductor to be examined, a new critical path being determined and optimized in each case (*id.*, col. 3, ll. 60-63).

The above optimization process yields a "secondary" network list that, in contrast to the primary (i.e., first) network list, contains the information which would be required by the person skilled in the art in order to adapt the cells in the layout to the optimized conditions, i.e., the additional dimensioning information for the components (*id.*, col. 3, l. 63 to col. 4, l. 2). However, the customary programs for synthesis of the CBN only generate CBNs with fixed references to specific standard cells which always have fixed dimensions (*id.*, col. 4, ll. 2-5).

Hatsch's improved method, in contrast, employs "parameterizable cells" (*id.*, col. 4, ll. 59-61), which are cells that "can grow or shrink practically in a continuously variable manner" (*id.*, col. 4, ll. 6-11).

Hatsch's method employs optimization that preferably has the following steps: (a) simulation of the integrated circuit using the primary network list; (b) discovery of a critical signal path in the simulated circuit;

and (c) optimization of the behavior of the critical signal path by variation of the component dimensions of the cells contained in it (*id.*, col. 7, ll. 54-61). Various optimization parameters can be used for optimizing the semiconductor, including, for example, "the *switching speed* of the integrated circuit, the area requirement of the circuit or the power loss of the circuit, in which case it is also possible for more than one optimization parameter to be used at the same time and it is possible to perform weighting in the consideration of the optimization parameters" (*id.*, col. 7, ll. 46-53) (emphasis added). Use of switching speed as an optimization parameter is also recited in Hatsch's claims 4 and 5 (*id.*, col. 14, ll. 9-12, 35-37).

Turning now to the question of obviousness, we agree with the Examiner that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of White and Hatsch by utilizing Hatsch's optimization parameter of switching speed in order to design a circuit with performance being the objective" (Answer 11). This obviousness rationale relies on Hatsch only for its teachings of designing an integrated circuit to satisfy a switching speed requirement and using switching speed as an electrical parameter for evaluating the performance of the actual structure predicted by a simulator. We agree with the Examiner that these teachings would have provided ample motivation to modify White's design method so as to employ switching speed as an electrical parameter for evaluating the actual structures predicted by White's simulator. This modification is not inconsistent with White's disclosure,

which characterizes the specific electrical parameters identified therein as exemplary by prefacing them with the term "e.g." *See* White at [0144] ("The . . . electrical characteristics (e.g. sheet rho variation, timing closure, signal integrity, power grid and overall performance) are checked 226 against specifications for the device.").

For the above reasons, we are unpersuaded by Appellants' argument that "[t]he Examiner has not provided reasons as to why White would use switching speed except the fact that another reference teaches switching speed" (Reply Br. 3) or by Appellants' other arguments to the same effect (*id.*). The rejection of claim 1 is therefore affirmed, as is the rejection of independent claim 31, as to which Appellants made the same arguments.

Inasmuch as we are affirming the rejection based on the above rationale, it is not necessary to address the Examiner's additional reliance on Hatsch's technique of optimizing critical paths (Answer 4[3]) or Appellants' criticisms of that reliance (Br. 4-6).

We are also affirming the rejection of claim 2, which depends on claim 1 and is not separately argued. *In re Young*, 927 F.2d 588, 590 (Fed.

[3] Specifically, the Examiner concluded that "[i]t would have been obvious to one of ordinary skill in the art to combine the teachings of White and Hatsch because adding Hatsch's desired characteristics of gain and/or switching speed would have improved White's system by optimizing layouts for functional capability and desired requirements concerning critical paths which would improve design and circuit performance [see Hatsch, col. 3, especially lines 1-16, and 43-51]." Answer 11 (brackets in original).

Cir. 1991). However, because Appellants are arguing the merits of claims that depend on claim 2, we note that it recites "determining actual dimensions of structures within the layout representation based on the simulating step" and "determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation."

Claim 3, which depends on claim 2, specifies that the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table. The Examiner reads this limitation on block 644 in White's Figure 25 and its associated paragraph [0211]. Answer 5; *id.* at 12 (*re* Argument 2a). Appellants correctly point out that neither block 644 (which is labeled "Use distortion (e.g. OPC) algorithms or look-up tables to compute the mapping between feature density and feature size variation") nor paragraph [0211] concerns electrical characteristics (Br. 7; Reply Br. 4). Nevertheless, we are affirming the rejection. White discloses using extraction and simulation tools to predict the electrical impact of feature width variations without giving the details of those tools (*see, e.g.*, paras. 0135, 0139, 0144-45, 0151, 0154). It would have been obvious in view of the look-up table described in paragraph [0211] to use a look-up table to determine the electrical characteristics from the dimensions of the structures predicted by the simulator. The rejection of claim 3 is affirmed.

Claim 4 depends on claim 2 and specifies that "the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input." Not only would it have been obvious in view of the algorithm described in paragraph [0211] to use an algorithm (i.e., a modeling program) to determine the electrical characteristics from the dimensions of the structures predicted by the simulator, White specifically discloses using a model for this purpose:

> [0306] The results of a layout extraction using the system are shown in the images in FIGS. 60A and 60 B. FIG. 60A shows a full-chip image 3167 of extracted feature widths (line widths in this case) across the chip according to the scale shown on the right 3168. In FIG. 60B, the spatial line widths across the full-chip are shown 3169, 3170, 3171, 3172, 3173, 3174 and 3175 according to which line width bin they fall into and useful distributions may be formed. This information, as well as line space, local and effective density may be input into the *models* to predict process and electrical variation.

[0306] (Emphasis added.)

The rejection of claim 4 is therefore affirmed.

Claim 6 depends on claim 1 and specifies that the step of generating a layout representation corresponding to the initial IC device design "includes minimizing the scale of the layout representation." The Examiner reads this limitation on paragraphs [0006-09, 0118, and 0137]. Answer 5; *id.* at 13 (*re* Argument 2c). Paragraph [0009] explains in pertinent part that "[i]mplementations of the invention may include one or more of the

following features. The generating is performed on sub-portions of the circuit." The Examiner's position is that generating adjusted designs on sub-portions of the circuit (layout) is a minimization of the scale of the original layout (Answer 13-14). Appellants have not pointed out any error in the Examiner's position, which strikes us as a reasonable one. Instead, Appellants simply summarize paragraph [0009] and assert that "[t]here is no language in the cited passage that teaches that the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation" (Br. 9), while the Reply Brief (at 5-6) discusses the other paragraphs relied on by the Examiner.

The rejection of claim 6 is therefore affirmed.

Claim 7 depends on claim 1 and specifies that "the initial IC device design includes a desired relationship between at least two structures within the IC device design." The Examiner reads this limitation on White's paragraphs [0006, 0015, 0118, and 0140-41]. Answer 5; *id.* at 14 (*re* Argument 2d). Of the cited paragraphs, the most relevant is [0118], which explains that

> [a] computer-aided-design (CAD) system 36 is used to translate a functional circuit design to an electronic layout design file that represents a physical device, layer-by-layer. The result is a design layout that describes each level of the device from the lowest level, for example a transistor level, up to higher levels, for example interconnect layers that transmit signals among transistors and supply power to the components on the chip.

This passage suggests that the functional circuit design, on which the Examiner reads the recited "initial IC device design" (Answer 3), contains information indicating which structures (e.g., transistors and interconnect lines) are connected to each other, which would appear to be enough to satisfy the claim. Appellants have not explained why the Examiner's reliance on paragraph [0118] is misplaced, instead simply asserting that "[t]here is no language in the cited passages that teaches that the initial IC device design includes a desired relationship between at least two structures within the IC device design" (Reply Br. 6). The rejection of claim 7 is therefore affirmed.

Claim 8 depends on claim 7 and calls for "determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design." The Examiner reads this limitation on paragraphs [0112-15, 0135, 0137-38, and 0140]. Answer 5; *id.* at 14-15 (*re* Argument 2e). Paragraph [0112] explains that the White patent "describe[s] approaches that are useful to identify and correct, in advance of lithographic mask creation, areas of an integrated circuit (IC) that are likely to be problematic due to variations in film thickness, surface topography uniformity, and electrical impact that arise in the manufacture of an integrated circuit." The claim language "process-related variation" is broad enough to read on any of these types of variations. Furthermore, because White's IC chips contain more than one structure, there will be amounts of these variations associated with at least two structures, as required by the

claim. Appellants' argument that "[t]here is no language in the cited passages that teaches determining an amount of process-related variation associated with at least two structures within the layout representation of the IC device design" (Br. 10) is not supported by an explanation of why the claim language cannot be read on White. The rejection of claim 8 is therefore affirmed.

The rejection of claim 9, which depends on claim 8 and is not separately argued, is also affirmed. However, because other argued claims depend on claim 9, we note that it specifies that the step (in claim 8) of determining an amount of process-related variation associated with at least two structures within the layout representation includes: "simulating how structures within the layout representation will pattern on a wafer; and measuring a feature of the simulated structures, said feature being indicative of process-related variation."

Claim 12 depends on claim 9 and calls for "measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity." We understand the term "window" in this claim to mean a "range." The Examiner reads this claim language on Figures 3 and 60A and corresponding paragraphs [0120-21, 0138, and 0306]. Answer 6; *id.* at 15 (*re* Argument 2f). Paragraph [0120], referring to Figure 3, explains that the projection system of the stepper adjusts so that the focal length 24 matches the measured distance to a test

key or alignment mark 26. This aspect of White's method is depicted in Figure 48, reproduced below.

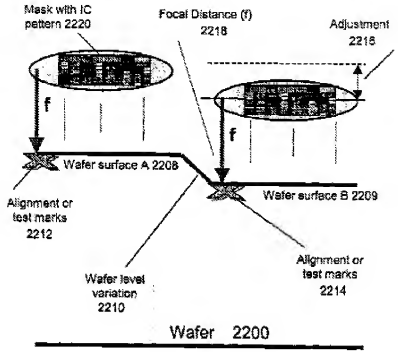

Fig. 48

Figure 48 shows a mask with an IC pattern 2220 to be imaged onto the wafer surface in areas A (2208) and B (2209), which have different heights and different alignment or test marks (2212, 2214) (*id.* at [0264]). We find that this adjustment process can accurately be characterized as including measurement (i.e., detection) of a feature (i.e., the test key or alignment mark) that is indicative of a process-related variation (i.e., a variation in topography) over a range of focus. Presumably the intensity (i.e., brightness) of the test key or alignment mark will vary with the distance between it and the lens during the adjustment operation. Appellants

have not explained why the claim language does not read on White in this way. Instead, they simply assert that "[t]here is no language in the cited passages that teaches measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity." Br. 11.

The rejection of claim 12 is therefore affirmed.

The rejection of claim 13, which depends on claim 12 and is not separately argued, is also affirmed.

Claim 14 depends on claim 1 and specifies that simulating how structures within the layout representation will pattern on a wafer (recited in claim 1)

> includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

The Examiner reads this claim language on White's Figure 25 and paragraphs [0112-14, 0133, 0138, 0211, and 0168]. Answer 6; *id.* at 15-16 (*re* Argument 2g[4]). Paragraph [0211], on which the Examiner (Answer 6) reads alternatives (ii) and (v), states the following:

> [0211] FIG. 25 describes the steps for mapping pattern feature densities to variation in lithography printed or imaged

[4] Mislabeled as argument 2f at line 1, page 16 of the Answer.

> feature dimensions 640. *Conventional optical proximity algorithms*, many of which are commercially available in EDA[5] tools, *are used to map feature density to feature dimension variation 644*. The computed feature dimension variation is at the layout feature resolution that is provided at both the layout resolution and extraction resolution 646. The resulting computation of feature dimension or feature width variation is then provided 740 to the verification component 800.

(Emphasis added.) Although Appellants have acknowledged that the Examiner relies on this paragraph for alternative (ii) (Br. 12), they have not acknowledged that this paragraph describes using commercially available EDA tools to map feature density to feature dimension variation or explained why that reliance is misplaced. Instead, their discussion of the content of paragraph [0211] is limited to denying that it satisfies alternative (v):

> Further, White instead teaches that the layout for the current design level is loaded and a table is assembled that maps layout features to discrete grids in chip surface topography prediction. [0211]. There is no language in the cited passages that teaches simulating how structures within the layout representation will pattern as a function of the size of a structure with respect to other adjacent structures.

Br. 12. The rejection of claim 14 is therefore affirmed.

The rejection is also affirmed with respect to unargued claims 15 and 16, which depend on claim 9.

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[5] "Electronics design automation" (White at [0006]).

Claim 17 depends on claim 16 and, further defines the modifying step recited in claim 1, which reads: "if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design. Claim 17 specifies the modifying step includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, and (ii) (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures. The Examiner reads alternatives (ii) and (v) on paragraph [0142] (Answer 7) and reads "one, if not all" of the alternatives on paragraphs [0112-15 and 0139-44]. Answer 17 (*re* Argument 2h).

> Paragraph [0142] explains by way of background that "dummy fill" is
>
> a method of improving film thickness uniformity in integrated circuits through the addition of the structures or the removal of existing structures. Adding metal dummy fill increases the pattern density since density is defined as the amount of metal divided by the total area within a given region. . . . By modifying the existing layout through the addition of dummy fill, physical parameters such as pattern density, line width, and line space are changed.

White, referring to blocks in White's Figure 10A, describes the use of dummy fill in White's invention as follows:

> [0141] The predicted feature dimension variation 680 and the desired feature dimension specification and tolerances 750 are input into a verification and correction component 800 which identifies any features that will exceed or approach the

> tolerances. This component also may be used to correct the dimensions of the identified features within the design layout and in subsequent mask creation so as to achieve the designed (or desired) feature dimensions across the chip. *Once these modifications are made to the IC design, dummy fill may be reinserted or adjusted and a new layout generated.*

(Emphasis added.)

Appellants argue that the dummy fill is not part of the "IC device design" and therefore does not satisfy claim 1, which calls for "modifying the initial IC device design:

> White teaches that after modifications are made to the IC design, dummy fill may be reinserted or adjusted where dummy fill improves film thickness uniformity. There is no language in the cited passage that teaches that if a portion of the IC device design is not optimized with respect to process-related variations, then a portion of the IC device design is modified by modifying the density of structures within a portion of the IC device design. Instead, White teaches that dummy fill may be reinserted or adjusted to improve film thickness uniformity after modifications are made.

Br. 13. Appellants appear to be arguing that dummy fill is not part of the active circuitry and thus not part of the "IC device design" of claim 1. However, Appellants have not explained, and is it not apparent, why the term "IC device design" is not broad enough to read on all of the structures represented by the layout, which White describes as including dummy fill:

> [0228] Verification results may be provided to the correction component 830, as illustrated in FIG. 30. In this component, modifications are computed for individual feature dimensions that exceed the design tolerances 832 and are used to physically

> modify feature dimensions in the electronic design layout to produce the desired printed or etched feature dimensions 920. *In certain cases, dummy fill or other geometries may need to be repositioned. The design layout is then re-generated 280 and if dummy fill is modified significantly, a new extraction performed.*

(Emphasis added.)[6]

The rejection of claim 17 is therefore affirmed.

Claim 18 depends on claim 9 and specifies that the process-related variations include variations caused by at least one of (i) mask generation, (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing. The Examiner reads claim 18 on paragraphs [0112-15, 0138, 0140, and 0147-49]. Answer 7; *id.* at 17-18 (*re* Argument 2i). Paragraph [0114] explains that "[i]n fabricating integrated circuits, the degree of interconnect film uniformity (in terms of both thickness and surface topography) is dependent on characteristics of circuit layout patterns (e.g. material density, line widths, line spaces, and other feature dimensions)." The term "wafer patterning" recited in alternative (ii) of the claim appears to be broad enough to read on these "circuit layout patterns" of line widths, line spaces, and other feature dimensions. Appellants have not explained why "circuit layout patterns" does not read on White in this way. The rejection of claim 18 is therefore affirmed.

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[6] The role of dummy fill in White's layout design is also depicted by blocks 2816, 2818, 2820, and 2822 in Figure 57, discussed in paragraphs
(Continued on next page.)

The rejection of claim 20, which depends on claim 1 and is not separately argued, is affirmed.

C. The merits of the rejection based on White in view of Hatsch and Rosenbluth

Claim 10 depends on claim 9, which as noted above, calls for "measuring a feature of the simulated structures, said feature being indicative of process-related variation." Claim 10 further specifies that the "feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity."

The dependency of claim 10 on claim 9 raises a question about how to construe those claims. The only example of slope edge intensity given in Appellants' Specification is "the slope[] of the *illumination* intensity at every edge of structures within the design" (Specification 12:3-5) (emphasis added). Although the illumination is used to produce a pattern representing the desired structures on the wafer (i.e., by exposing a photoresist – Specification 1:16-26), the illumination itself would not ordinarily be considered "a feature of the . . . structures," as required by claim 9. However, because the only example of slope of intensity given in the Specification is slope of illumination intensity, we understand the phrase "a feature of the simulated structures" in claim 9 to be broad enough to read on features of the process used to simulate the structures.

[0300-02].

Rosenbluth explains that when the critical dimensions (CDs) of a desired IC pattern approach the resolution of a lithographic system (defined as the smallest dimensions that can be reliably printed by the system), image distortions become a significant problem (Rosenbluth [0002]). Rosenbluth's invention is a method for selecting and using combinations of illumination source characteristics and diffracting shapes on a reticle mask in order to project and print an image on a semiconductor wafer that substantially matches the shape of the desired IC patterns with minimal distortion (*id.* at [0001]).

Rosenbluth "Background of the Invention" describes a number of known techniques to compensate for the image degradation that occurs when the resolution of optical lithography systems approaches the critical dimensions of desired lithographic patterns that are used to form devices and ICs on a semiconductor chip (*id.* at [0002]). A technique known as "phase-shifting chrome" or "attenuated phase shift" improves image sharpness by augmenting the rate of change in illumination amplitude across the edge of mask features (*id.* at [0015]). This is achieved by using a phase-shifting material of slightly negative transmittance for dark areas of the pattern, rather than the conventional material of zero transmittance (*id.*). Phase shifting increases the slope of illumination intensity at the edges of image features because the transmitted electric field makes a transition from unity to a value less than zero, as shown for example by waveform 160 in Figure 1A (*id.*).

The so-called alternating-phase-shift achieves contrast improvement by successively shifting the phase of adjacent bright features between 0 and 180° (*id.* at 0016]).

It is also known to select the illumination directions incident on a given mask in ways that maximize the slope of image features and to minimize critical dimension nonuniformity between different features through superposition of multiple illumination directions (*id.* at [0019]).

Rosenbluth's method achieves enhancement of the image with respect to a desired IC pattern by simultaneously choosing parameters of source illumination and mask transmission features in a lithographic imaging system so that features of the projected image are optimized as measured by a merit function in accordance with a set of constraints on the image features and lithographic process parameters (*id.* at [0061]).

Rosenbluth's Figure 5 is reproduced below.

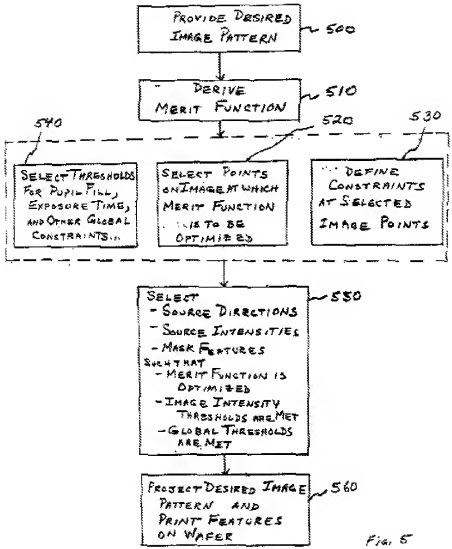

Fig. 5

Figure 5 is a flow chart of an embodiment of Rosenbluth's invention (*id.* at [0061]).

A merit function based on the image intensity may be defined in terms of unknown values of source directions and intensities and diffracted wavefront amplitudes expressed as diffraction order amplitudes using

standard equations of image formation which are based on well known principles of optics (*id.* at [0063]). In one embodiment, a merit function is chosen that describes the gradient of the image across the edges of features at selected critical positions such that the smallest slope at all selected positions is maximized (*id.*).

The merit function can be maximized (block 550 in Fig. 5) to solve for the unknown source directions and intensities and diffraction order amplitudes using standard techniques for global optimization that are known in the art (*id.* at 0065]). The resulting optimized source directions, source intensities, and diffracted wave front (or diffraction order) amplitudes are then implemented within a lithographic system, while the reticle mask features corresponding to the derived optimal diffraction order amplitudes may be readily determined, since the relationship between diffraction pattern and reticle transmittance is linear, based on a Fourier transform (*id.*).

In one embodiment, Ψ is a merit function that represents the worst-case log-slope arising at feature edges in the image (*id.* at [0082]). Optimization of Ψ ensures that the shallowest slope among feature edges is as steep as possible (*id.*). Optimization using the log-slope is discussed in [0099].

The Examiner found that the slope of illumination intensity described in Rosenbluth is subject to and therefore "indicative of process-related variation" in the sense of claim 10. *See* Answer 20 ("The slope edge intensities are part of a lithography process used in manufacturing integrated

circuits"); *id.* at 21 ("Slope edge intensities, and logarithms of the slope edge intensities are process related variations that result from the imaging of features of an integrated circuit during the design and/or the manufacture of integrated circuits or masks . . . ."). Appellants have not pointed out any error in this position of the Examiner. That is, they have not specifically explained which claim terminology is not satisfied and why. Instead, they simply summarize the contents of Rosenbluth's paragraphs [0115, 0019, and 0099] and assert that "[t]here is no language in the cited passages that teaches that the feature of the simulated structures indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity" (Br. 18-19).

Turning now to the Examiner's rationale for combining the reference teachings, the Examiner concluded that

> [i]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of White in view of Hatsch with the method disclosed by Rosenbluth because such combined method includes slope of edge intensity / logarithm of slope of edge intensity [and] would provide a technique for optimally choosing illumination distribution and mask features (paragraph [0021]).

Answer 10. The foregoing rationale strikes us as a straightforward case of combining two different methods in order to obtain the benefits of both. That is, White's method of designing layouts for masks fails to take into account the types of image distortion that Rosenbluth explains are encountered when the resolution of optical lithography system approaches

the critical dimension of the desired lithographic pattern (Rosenbluth at [0015]). Rosenbluth's method solves these problems by ensuring that the shallowest slope among feature edges is as steep as possible (*id.* at [0082]) and by appropriate design of the reticle mask features (*id.* at [0065]). Consequently, we do not agree with Appellants' argument that the Examiner failed to provide any rationale for combining the reference teachings (Reply Br. 13).

Nor are we persuaded by Appellants' argument that "White is not concerned with optimally choosing illumination distribution and mask features" (Br. 17). While it is true that a prior art teaching away from a combination makes that combination more likely to have been nonobvious *KSR*, 127 S. Ct. at 1739-40, White's failure to disclose optimizing the illumination distribution does not teach away from modifying White to include such optimization. *See In re ICON Health and Fitness, Inc.*, 496 F.3d 1374, 1381 (Fed. Cir. 2007) ("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.") (citations omitted).

We are therefore affirming the rejection of claim 10.

Claim 11 depends on claim 10 and specifies that "a larger slope of edge intensity or logarithm of slope of edge intensity is indicative of a smaller process-related variation; and a smaller slope of edge intensity or

logarithm of slope of edge intensity is indicative of a larger process-related variation." Due to it dependency on claim 9 through claim 10, it is necessary for the inverse relationships recited in claim 11 to be used to "determin[e] an amount of process-related variation" (claim 9). Regarding claim 11, the Examiner cites Rosenbluth's paragraphs [0002, 0015, 0019, 0082 and 0099] (Answer 20-21). Appellants correctly note (Br. 19; Reply Br. 12-14) that these paragraphs do not describe the claimed inverse relationship between the amount of the slope (or its logarithm) and the amount of process-related variation and thus do not suggest using the inverse relationships recited in claim 11 to determine an amount of process-related variation.

We are therefore reversing the rejection of claim 11 and its dependent claim 19.

CONCLUSIONS OF LAW

Appellants have not shown reversible error in the rejection of claims 1-4, 6-9, 12-18, 20, and 31 under 35 U.S.C. § 103(a) for obviousness over White in view of Hatsch. Nor have Appellants shown reversible error in the § 103(a) rejection of claim 10 for obviousness over White in view of Hatsch and Rosenbluth.

However, Appellants have shown reversible error in the § 103(a) rejection of claims 11 and 19 for obviousness over White in view of Hatsch and Rosenbluth.

DECISION

The Examiner's decision that claims 1-4, 6-20, and 31 are unpatentable over the prior art is therefore affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. §§ 41.50(f) and 41.52(b) (2008).

AFFIRMED-IN-PART

rvb

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